Knowledge Network of
Indian Institute of Technology, Gandhinagar
Under TEQIP-II Initiative (MHRD, Govt. of Gujarat)

Workshop on
The Art of Compact Modeling

Date:	12-21 May 2014 (8-days, leave on 17-18 May)
Time:	10:00am to 5:00pm
Venue:	IIT Gandhinagar Shed-5
Target group:	Faculty members and graduate students
Register At:	www.iitgn.ac.in/kn
Deadline:	5 May 2014

Compact Models of circuit elements (like resistors, diodes, varactors, MOS capacitors and transistors) are models that are sufficiently simple to be incorporated in circuit simulators and at the same time sufficiently accurate to make the outcome of the circuit simulation useful for the circuit designers. The conflicting objectives of model simplicity and accuracy make the compact modeling field an exciting and challenging research area for device physicists, modeling engineers and circuit designers.

The models of semiconductor devices underwent revolutionary change in the last few years and are now based on new principles. The recent models of diodes, passive elements, noise sources and MOS transistors were developed along the more traditional lines. Following this evolutionary development they became highly sophisticated and much more capable to reflect the increased demands of the advanced integrated circuit technology. The latter depends on the compact models for the shortening of the design cycle and eliminating the elements of overdesign which is often undesirable in today's competitive environment. At the same time, statistical modeling of semiconductor devices received new significance following the dramatic reduction of the device dimensions and of the power supply voltage.

This course will cover the techniques generally used for compact modeling of semiconductor devices. The detailed device physics behind the operation of semiconductor diodes, capacitors and transistors will also be discussed.
